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Claims

[c1] 1. A source driver, receiving a clock signal, a display data, and a control signal to drive a display panel, comprising:
a receiver for receiving said clock signal, said display data, and said control signal; and
a transmitter, coupled to said receiver, for enhancing a driving ability of said clock signal, said display data, and said control signal and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of another source driver in a next stage.

[c2] 2.The source driver of claim 1, wherein said transmitter is a differential signal transmitter.

[c3] 3.The source driver of claim 2, wherein said receiver is a differential signal receiver.

[c4] 4. The source driver of claim 2, wherein said transmitter is a voltage mode differential signal transmitter.

[c5] 5. The source driver of claim 2, wherein said transmitter is a current mode differential signal transmitter.

[c6] 6.The source driver of claim 1, wherein said transmitter is a TTL signal transmitter.

[c7] 7. The source driver of claim 6, wherein said receiver is a TTL signal receiver.

[c8] 8. The source driver of claim 1, wherein said transmitter includes:
a data synchronization circuit synchronizing said clock signal, said display data, and said control signal received from said receiver; and
a plurality of buffers, coupled to said data synchronization circuit, receiving said synchronized clock signal, said synchronized display data, and said synchronized control signal, enhancing said driving ability of said synchronized clock signal, said synchronized display data, and said synchronized control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c9] 9. The source driver of claim 1, wherein said transmitter includes a plurality of voltage buffers receiving said clock signal, said display data, and said control signal, enhancing said driving ability of said clock signal, said display data, and said control signal, and outputting said enhanced clock signal, said enhanced display data, and

said enhanced control signal for use of said another source driver in said next stage.

[c10] 10.The source driver of claim 1, wherein said display panel is a α-Si liquid crystal display panel.

[c11] 11.The source driver of claim 1, wherein said display panel is a low temperature poly-silicon liquid crystal display panel.

[c12] 12.A flat panel display, comprising:
a display panel;
a timing controller outputting a clock signal, a display data, and a control signal; and
a plurality of source drivers, said plurality of source drivers being series-connected to be a series structure, said plurality of source drivers being coupled to said display panel, one end of said series structure being coupled to said timing controller, said plurality of source drivers receiving said clock signal, said display data, and said control signal to drive said display panel, enhancing a driving ability of said clock signal, said display data, and said control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of another source driver in a next stage.

[c13] 13. The flat panel display of claim 12, wherein each of said plurality of source drivers, comprises:
a receiver for receiving said clock signal, said display data, and said control signal; and
a transmitter, coupled to said receiver, for enhancing said driving ability of said clock signal, said display data, and said control signal and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c14] 14.The flat panel display of claim 13, wherein said transmitter is a differential signal transmitter.

[c15] 15.The flat panel display of claim14, wherein said receiver is a differential signal receiver.

[c16] 16. The flat panel display of claim14, wherein said transmitter is a voltage mode differential signal transmitter.

[c17] 17. The flat panel display of claim 14, wherein said transmitter is a current mode differential signal transmitter.

[c18] 18.The flat panel display of claim13, wherein said transmitter is a TTL signal transmitter.

[c19] 19. The flat panel display of claim18, wherein said re-

ceiver is a TTL signal receiver.

[c20] 20. The flat panel display of claim 13, wherein said transmitter includes:
a data synchronization circuit synchronizing said clock signal, said display data, and said control signal received from said receiver; and
a plurality of buffers, coupled to said data synchronization circuit, receiving said synchronized clock signal, said synchronized display data, and said synchronized control signal, enhancing said driving ability of said synchronized clock signal, said synchronized display data, and said synchronized control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c21] 21. The flat panel display of claim13, wherein said transmitter includes a plurality of voltage buffers receiving said clock signal, said display data, and said control signal, enhancing said driving ability of said clock signal, said display data, and said control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c22] 22.The flat panel display of claim12, wherein said dis-

play panel is a α-Si liquid crystal display panel.

[c23] 23.The flat panel display of claim12, wherein said display panel is a low temperature poly-silicon liquid crystal display panel.

[c24] 24. A source driver, receiving a master/slave setting signal, a clock signal, a display data, and a control signal to drive a display panel, comprising:
a receiver for receiving said clock signal, said display data, and said control signal; and
a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter operates in said master mode, said transmitter enhances a driving ability of said clock signal, said display data, and said control signal and outputs said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of another source driver in a next stage; when said transmitter operates in said slave mode, said transmitter directly outputs said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage.

[c25] 25.The source driver of claim 24, wherein said transmit-

ter is a differential signal transmitter.

[c26] 26.The source driver of claim 25, wherein said receiver is a differential signal receiver.

[c27] 27. The source driver of claim 25, wherein said transmitter is a voltage mode differential signal transmitter.

[c28] 28. The source driver of claim 25, wherein said transmitter is a current mode differential signal transmitter.

[c29] 29.The source driver of claim 24,wherein said transmitter is a TTL signal transmitter.

[c30] 30. The source driver of claim 29, wherein said receiver is a TTL signal receiver.

[c31] 31. The source driver of claim 24, wherein said transmitter includes:

a data synchronization circuit synchronizing said clock signal, said display data, and said control signal received from said receiver; and

a plurality of buffers, coupled to said data synchronization circuit, receiving said synchronized clock signal, said synchronized display data, and said synchronized control signal, enhancing said driving ability of said synchronized clock signal, said synchronized display data, and said synchronized control signal, and outputting

said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c32] 32. The source driver of claim 24, wherein said transmitter includes a plurality of voltage buffers receiving said clock signal, said display data, and said control signal, enhancing said driving ability of said clock signal, said display data, and said control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c33] 33.The source driver of claim 24, wherein said display panel is a α-Si liquid crystal display panel.

[c34] 34.The source driver of claim 24, wherein said display panel is a low temperature poly-silicon liquid crystal display panel.

[c35] 35.A flat panel display, comprising:
a display panel;
a timing controller outputting a clock signal, a display data, and a control signal;
a control circuit outputting a plurality of mater/slave setting signals; and
a plurality of source drivers, said plurality of source

drivers being series-connected to be a series structure, said plurality of source drivers being coupled to said display panel, one end of said series structure being coupled to said timing controller, said plurality of source drivers receiving said clock signal, said display data, and said control signal to drive said display panel, each of said plurality of source drivers responsive to a corresponding one of said plurality of mater/slave setting signals determining whether to enhancing a driving ability of said clock signal, said display data, and said control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of another source driver in a next stage.

[c36] 36. The flat panel display of claim 35, wherein each of said plurality of source drivers, comprises:
a receiver for receiving said clock signal, said display data, and said control signal; and
a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter operates in said master mode, said transmitter enhances said driving ability of said clock signal, said display data, and said control signal and outputs said enhanced clock signal, said enhanced

display data, and said enhanced control signal for use of said another source driver in said next stage; when said transmitter operates in said slave mode, said transmitter directly outputs said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage.

[c37] 37.The flat panel display of claim36, wherein said transmitter is a differential signal transmitter.

[c38] 38.The flat panel display of claim37, wherein said receiver is a differential signal receiver.

[c39] 39. The flat panel display of claim37, wherein said transmitter is a voltage mode differential signal transmitter.

[c40] 40. The flat panel display of claim 37, wherein said transmitter is a current mode differential signal transmitter.

[c41] 41.The flat panel display of claim36, wherein said transmitter is a TTL signal transmitter.

[c42] 42. The flat panel display of claim41, wherein said receiver is a TTL signal receiver.

[c43] 43. The flat panel display of claim 36, wherein said transmitter includes:
a data synchronization circuit synchronizing said clock

signal, said display data, and said control signal received from said receiver; and

a plurality of buffers, coupled to said data synchronization circuit, receiving said synchronized clock signal, said synchronized display data, and said synchronized control signal, enhancing said driving ability of said synchronized clock signal, said synchronized display data, and said synchronized control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c44] 44. The flat panel display of claim36, wherein said transmitter includes a plurality of voltage buffers receiving said clock signal, said display data, and said control signal, enhancing said driving ability of said clock signal, said display data, and said control signal, and outputting said enhanced clock signal, said enhanced display data, and said enhanced control signal for use of said another source driver in said next stage.

[c45] 45.The flat panel display of claim35, wherein said display panel is a α-Si liquid crystal display panel.

[c46] 46.The flat panel display of claim35, wherein said display panel is a low temperature poly-silicon liquid crystal display panel.